VHDL Implementation of Reed-Solomon Encoder-Decoder for WiMax Network

Ranjita Singh[1]
ranjiricha@gmail.com

Krikshankant Pathak[2]
kk_sonu@yahoo.com

Ece Department,
Techno Craft Institute Of
Technology, Bhopal, India

Abstract— **This article proposes, a system based on Reed-Solomon codec for WiMax networks. The proposed architecture implements various programmable primitive polynomials. A lot of VLSI implementations have been described in literature. This paper introduces a highly parametrical RS-coder-decoder. The implementation, written in a hardware description language (HDL), is based on an Berlekamp massey, Chien Search and Formey Algorithms. Wehave defined an advanced RS encoder-decoder architecture approach whichis a key solution for systems. Our approach is used inorder to implement on Xilinx a generic RS coder-decoder for WiMax networks. IEEE Std.802.16 specifies that the codec performs a variable number of check symbols in a codeword. The Reed-Solomon encoder has been checked for different error-correcting capabilities that is 4, 6, 8 etc. Reed-Solomon decoder synthesized using VHDL on Xilinx and simulated on ISE Simulator.The RS decoder implementation written in VHDL is based on Berlekamp Massey,Forney and Chien Search Algorithm. The performance of Reed-Solomon encoder RS (7,3)and,RS(15,9) is shown and Reed-Solomon decoder is checked for RS(7,3)and synthesizable on Xilinx and simulated on ISE Simulator. The performance are shown using two device Virtex 5 and Spartan 3e.**

Index Terms— Reedsolomon, Berlekamp massey, Chien, Forney, implementation, VHDL, WiMax,

1. INTRODUCTION

Reed-Solomon (RS) codes first appeared in technical literature in 1960. In 1960 Irving S**.** Reed and Gustave Solomon, staffmembers at MIT's Lincoln Laboratory[1], developed the Reed-Solomon code, which has become the most widely used algorithm for error correction. RS are powerful error correcting codes that can be employed in a wide variety of digital communications systems from digital media to wireless communications and deep-space probes as well as in memory and storage systems. Reed-solomon codes are used to correct errors in many systems including:

- storage devices (compact disk, DVD, barcodes,etc….) [2,3],
- wireless and mobile communications (including cellular telephones, microwave links, etc…)[4, 5],
- digital satellite communications[6],
- digital television, digital video broadcasting (DVB)[7],
- high speed modem such as ADSLXdsl…[8]
- power line communications (PLC) [9]
- digital vestigial sideband (VSB) system[10],

They are use in a variety of applications.These applications include CD audio players, medical diagnosis military purposes and countless wired . RS codes belong to the family of block codes. Block code is so named because the encoder processes a block of message symbols and then outputs a block of codeword symbol. RS codes are non-binary systematic cyclic linear block codes. Non-binary codes work with symbols that consist of several bits. A common symbol size for non-binary codes is 8 bits, or a byte. Non-binary codes such as RS are good at correcting burst errors because the correction of these codes is done on the symbol level, these codes can correct a symbol with a burst of eight errors just as easily as they can correct a symbol with a single bit error. The encoder applies a reversible mathematical function to the message symbols in order to generate the redundancy, or parity, symbols. The codeword is then formed by appending the parity symbols to the message symbols. The implementation of a code is simplified if it is systematic .implementations of RS codes have been published over the years targeting ASIC, FPGA, or DSP applications . Reed-Solomon codes are based on the finite fields so they can be extended or shortened. In this paper Reed-Solomon codes implemented for using VHDL codes. The generator polynomial approach has been used for encoding and decoding of Data.

2. REED-SOLOMON CODE

Reed Solomon (RS) codes are a subset of Bose Chaudhuri-Hochquenghem (BCH) codes [21 22] and are linear block codes[23]. Their non-binary nature makes them particularly suitable to correct error bursts. A Reed-Solomon code is a block code and can be specified as RS (n,k) as shown in Figure 2.1.

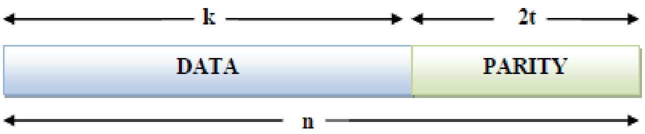


Figure 2.1: Structure of a RS codeword

RS codes are generally represented as an RS (n, k), with m-bit symbols, where

- Block Length : n
- No. of Original Message symbols: k
- Number of Parity Digits: n - k = 2t
- Minimum Distance: d = 2t + 1.

The relationship between the symbol size, m, and the size of the codeword n, is given by

$n = 2^m - 1$

Code generator polynomial:

g(x) = (x+µ0) (x+µ1) (x+µ2) ... (x+µ2t-1), where µ= 02hex (3)

Field generator polynomial:

p(x) = x8 + x4 + x3 + x2 + 1

2.1 Generator polynomial of a Reed-Solomon code

A Reed Solomon code is a special case of a BCH code in which the length of the code is one less than the size of the field over which the symbols are defined. It consists of sequences of length (q – 1) whose roots include 2t consecutive powers of the primitive element of GF(q). Alternatively, the Fourier transform over GF(q) will contain 2t consecutive zeros. Note that because both the roots and the symbols are specified in GF(q), the generator polynomial will have only the specified roots; there will be no Conjugates. Similarly the Fourier transform of the generator sequence will be zero in only the specified 2t consecutive positions.

A consequence of there being only 2t roots of the generator polynomial is that there are only 2t parity checks. This is the lowest possible value for any t-error correcting code and is known as the Singleton bound. To construct the generator for a Reed Solomon code, we need only to construct the appropriate finite field and choose the roots. Suppose we decide that the roots will be from αi to αi+2t-1, the generator polynomial will be,

$$g(X) = (x+\alpha^{i})(x+\alpha^{i+1})\dots(x+\alpha^{i+2t-2})(x+\alpha^{i+2t-1})$$

In contrast to the case with binary BCH codes, the choice of value of i will not affect the dimension or the minimum distance of the code because there are no conjugates to consider [10].

2.2 Encoding of Reed-Solomon Codes

The Reed-Solomon encoder reads in k data symbols, computes the n - k parity symbols, and appends the parity symbols to the k data symbols for a total of n symbols. The encoder is essentially a 2t tap shift register where each register is m bits wide. The multiplier coefficients are the coefficients of the RS generator polynomial. The general idea is the construction of a polynomial; the coefficients produced will be symbols such that the generator polynomial will exactly divide the data/parity polynomial. The transmitted codeword is systematically encoded and defined in as a function of the transmitted message m(x), the generator polynomial g(x) and the number of parity symbols 2t as given below.

c(x)=m(x) * 2t + m(x)modg(x)

Where, g(x) is the generator polynomial of degree 2t and given by,

$$g(x) = \prod_{i=m_0}^{m_0+2t-1} (x+\alpha^{i})$$

2.3 Decoding of Reed-Solomon codes

The general decoding steps are illustrated in Figure 3. The syndrome calculator generates a set of syndromes from the received codeword polynomial R(x). From the syndromes, the key equation solver produces the error locator polynomial and the error evaluator polynomial which can be used by the Chien Search and the Error Value Evaluator to determine the error locations and error values, respectively.

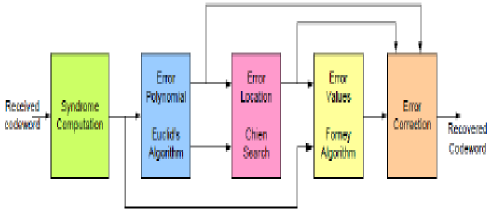


Fig.2.2. General Architecture of RS Decoder

3 RS DECODING ALGORITHMS

3.1 Syndrome computation

The Syndrome calculation block treats the input codeword as a series of polynomial coefficients and calculates a syndrome polynomial of 2t coefficients. The syndrome polynomial contains the location and magnitude of up to t errors in an invalid codeword. A valid codeword generates a syndrome polynomial with all zero coefficients. This is a similar calculation to parity calculation. The syndromes can be calculated by substituting the 2t roots of the generator polynomial g(x) into r(x).Syndrome is calculated to check the presence of errors at the receiver end. If the error correction capability of code is 8 then syndromes will be 16 that is 2t. The syndrome polynomial contains the location and magnitude of up to t errors in an invalid codeword. A valid codeword generates a syndrome polynomial with all zero coefficients.

3.1Berkelamp-Massey algorithm

The Berlekamp–Massey algorithm is an alternate iterative procedure for finding the error locator polynomial. During each iteration, it calculates a discrepancy based on a current instance of Λ(x) with an assumed number of errors *e* and then adjusts Λ(x) and *e* so that a recalculated Δ would be zero.

3.2 chien search and error -correction

Chien search is used to find the roots of polynomial in reed-solomon decoder. Chien search performs the function of finding the error locations, and correcting the data.When the Chien sum is zero,Forney algorithm is used. Chien search uses all possible input values and then checks to see if the outputs are zero. In the reed-solomon decoder, the delay block is the necessary to adjust for the delays in the syndrome block and startup delay in the Chien search block. The block diagram for Reed-Solomon decoder.

3.3Forney Algorithm

The Forney algorithm is used to compute the error values *Yi*. To compute these values, the Forney algorithm needs the error locator polynomial *(x) and error* magnitude polynomial Ω(x).

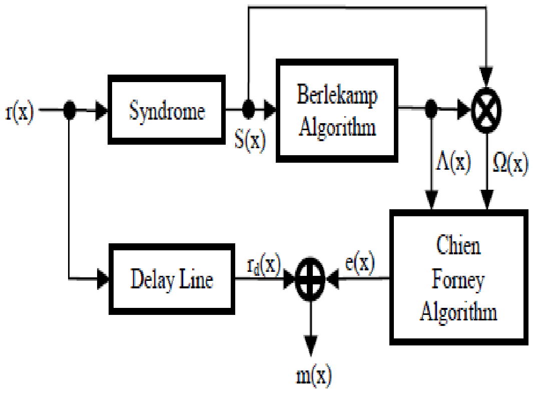


Fig.3.1. Block Diagram Of Reed-Solomon Decoder

4. RS PARAMETERIZATION FOR WIMAX NETWORK

IEEE 802.16 Network is called as Wimax network IEEE Std. 802.16 specifies the outer code requirements for RS code as follows:

The specified code generator polynomials are given by:

- *Code Generator Polynomial:*

$g(x) =(x+\mu 1)(x+\mu 2) \ldots (x+\mu 2T)$, where μ=02hex

- *Field Generator Polynomial:*

$p(x) = x8 + x4 + x3 + x2 + 1$

Different parameters can have generic value in configurable RS module.

Fully parameterized RS function, including:

- Number of bits per symbol
- Number of symbols per codeword
- Number of check symbols per codeword
- Field polynomial
- First root of generator polynomial

5. IMPLEMENTATION

Reed-Solomon code is written in VHDL on Xilinx 12.1 and simulated in ISE simulator and synthesizable on Virtex 5and Spartan 3e. Reed Solomon codes are implemented to reduce the hardware complexity and utilization.

5.1 Encoder Implementation

Reed-Solomon encoder for RS(7,3)and,Rs(15,9) are implemented in VHDL to encode the data symbols for reliable communication. The register transfer level (RTL) for this code are shown in figure .The RTL view technology for this code are shown in figure.

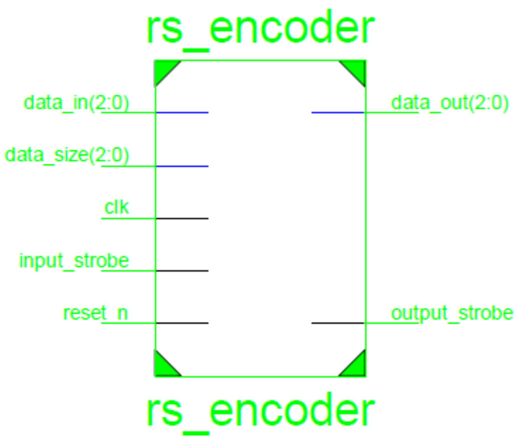


Fig5.1. RTL schematic symbol for RS(7,3) encoder

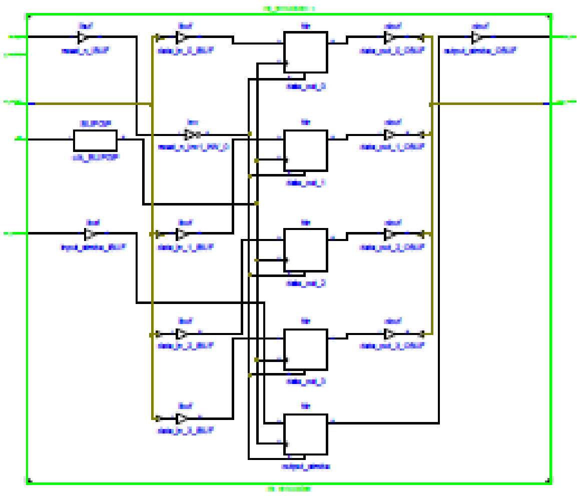


Fig.5.2 RTL View Technology for RS(7,3) Encoder for WiMax Network

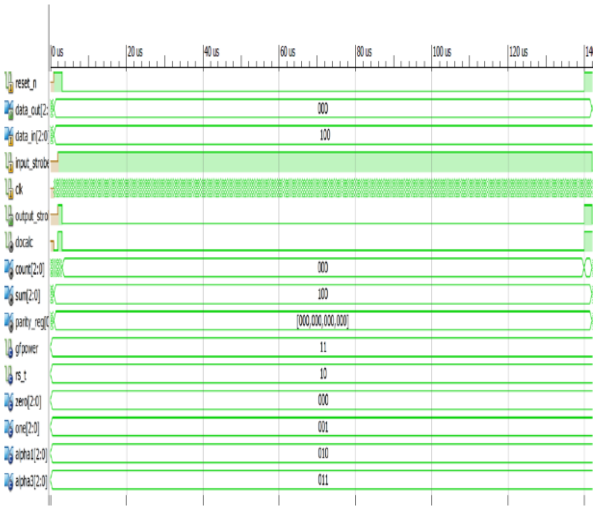


Fig 5.3 Simulation result of RS(7,3) Encoder

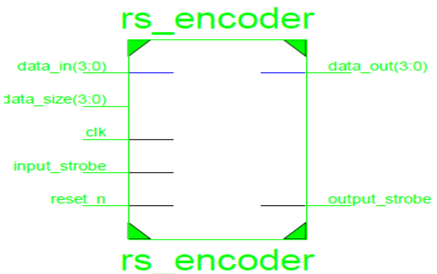


Fig.5.4. RTL Schematic Symbol for RS(15,9) Encoder

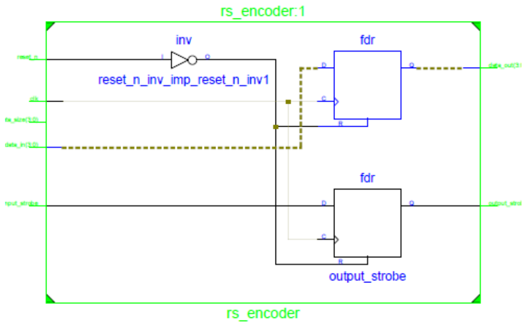


Fig.5.5 RTL View Technology for RS(15,9)

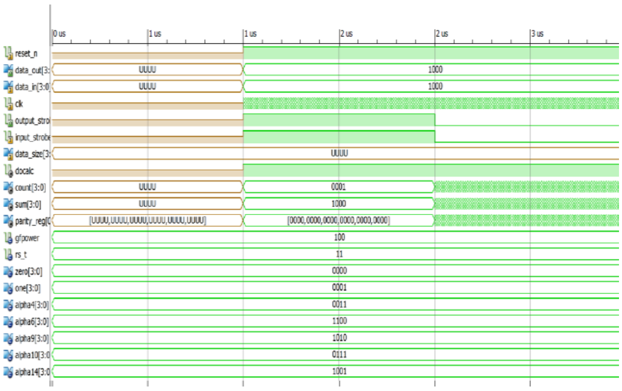


Fig.5.6 Simulation result of RS(15,9) Encoder for WiMax Network

5.2 Decoder Implementation

Reed-Solomo Decoder for RS(7,3) is implemented in VHDL on Xilinx 12.1synthesized on Virtex 5 and Spartan 3e.

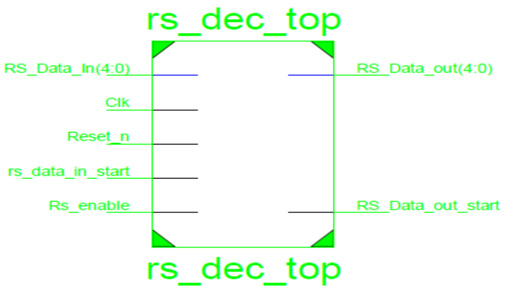


Fig.5.7. RTL Schematic Symbol for RS(7,3) Decoder

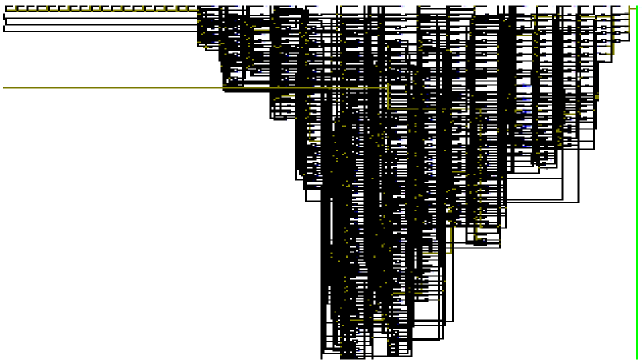
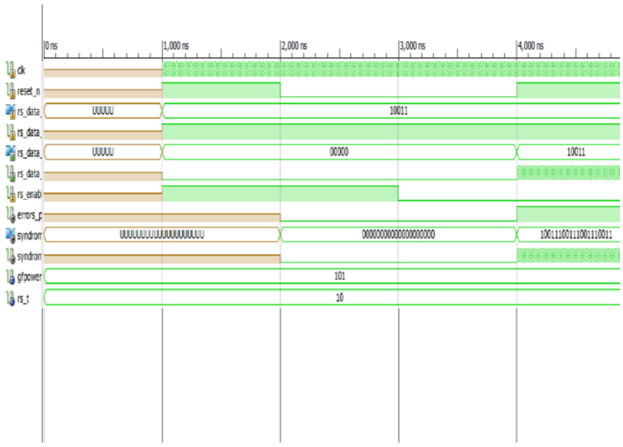


Fig.5.8 RTL View of RS(7,3) Decoder



5.9 Simulation result of RS(7,3) Decoder

6. FPGA IMPLEMENTATION RESULT

The Reed-Solomon Encoder and Decoder are synthesized using Xilinx Virtex5 FPGA to measure the performance of the implemented RS code,which is compared to the performance of the Reed-Solomon code provided by Xilinx Spartan 3e FPGA.The performance comparision in terms of resource utilization of FPGA are Shown in Table I,Table II, and Table III.

Table.I: Resource utilization on Xilinx Virtex 5 and Spartan 3e FPGA For RS (15,9) Encoder.

FPGA Device	**Virtex 5(xc5vix50t-3ff1136)**		**Spartan 3e(xc3s500e-4-fg-320)**	
Resource Type	**Used**	**ratio**	**Used**	**Ratio**
Number of bonded IOBs	**12 out of 480**	**2%**	**12 out of 232**	**5%**
IOB Flip Flops	**5**		**5**	
Number of BUFG/BUFGCTRLs	**1 out of 32**	**3%**	**1 out of 24**	**4%**
Average Fanout of Non-Clock Nets	**0.92**		**0.83**	

Table.II: Resource utilization on Xilinx Virtex 5 and Spartan 3e FPGA For RS (7,3) Encoder.

FPGA Device	**Virtex 5(xc5vix50t-3ff1136)**		**Spartan 3e(xc3s500e-4-fg-320)**	
Resource Type	**Used**	**ratio**	**Used**	**ratio**
Number of Slice Flip Flops	**19 out of 28800**	1%	**19 out of 9312**	1%
Number of 4 input LUTs	**24 out of 28800**	1%	**25 out of 9312**	1%
Number of occupied Slices	**8 out of 7200**	1%	**17 out of 4656**	1%
Number of Slices containing only related logic	**24 out of 28800**	1%	**17 out of 17**	**100%**
Number of bonded IOBs	**13 out of 480**	2%	**13 out of 232**	5%
IOB Flip Flops	**1**		**1**	
Number of BUFGMUXs	**1 out of 32**	3%	**1 out of 24**	4%
Average Fanout of Non-Clock Nets	**3.54**		**2.79**	
Number of BUFGMUXs	**1 out of 32**	3%	**1 out of 24**	4%

Table.III: Resource utilization on Xilinx Virtex 5 and Spartan 3e FPGA For RS (7,3) Decoder.

FPGA	**Virtex5(xc5vix50t-3ff1136)**		**Spartan 3e(xc3s500e-4-fg-320)**	
Resource Type	**Used**	**ratio**	**Used**	**ratio**
Number used as Flip Flops	**194 out of 28800**	1%	**194 out of 9312**	2%
Number of Slice LUTs	**234 out of 28800**	1%		
Number used as logic	**229 out of 28800**	1%	**332**	
Number used as Shift Register	**5**		**10**	
Number of occupied Slices	**110 out of 7200**	1%	**223 out of 4656**	4%
Number of bonded IOBs	**15 out of 480**	3%	**15 out of 232**	6%
Number used as BUFGs	**1 out of 32**	3%	**1 out of 24**	4%
Average fan out of Non-Clock Nets	**4.42**		**3.75**	

7. CONCLUSION

This paper implements the Reed-Solomon code RS(7,3) and Rs(15,9). The decoder checks the received data for any errors by calculating the syndrome of the codeword. If an error is detected, the process of correction begins by locating the errors first. Generally Euclid's Algorithm is used to calculate the error – locator polynomial it is very easy to implement, while its counterpart Berlekamp - Massey Algorithm is more hardware efficient. The precise location of the errors is calculated by using Chien search algorithm. Then magnitude of the errors is calculated using Forney's algorithm. The magnitude of the error is added to the received codeword to obtain a correct codeword. Hence the using the Reed – Solomon codes, burst errors can be effectively corrected. This represents reduction in the cost and save a lot of area. Reed-Solomon encoder RS(7,3) and RS(15,9) are implemented to encode the data symbols. The code is implemented in VHDL on Xilinx 12.1 and synthesized on Virtex and Spartan 3e for WiMax Network.

8. ACKNOWLEDGEMENT

The author would like to thank Rajiv Gandhi University for providing this opportunity to do work in this field. And also want to thank faculty members for continuous support and encouragement.

REFERENCES

[1] I. S. Reed and G. Solomon, " Polynomial codes over certain finite fields", *Journal of the Society for Industrial and Applied Mathematics*, 8:300-304, 1960.

[2] T. R. N. Rao and E. Fujiwara, Error Control Coding for Computer Systems, *Prentice-Hall, Englewood Cliffs, NJ, USA*, 1989.

[3] H.C.Chang, C.B.Shung, CY.Lee, "A Reed- Solomon product-code (RS-PC) decoder chip for DVD applications", *Solid-State Circuits, IEEE Journal* , Volume: 36 Issue: 2 , Feb. 2001 Page(s): 229 –238.

[4] Y.Cho, K.Kang, J.Lee and H.Shin "Proactive Reed-Solomon Bypasss (PRSB): A Technique for Real-Time Multimedia Processing in 3G Cellular Broadcast Networks", *The 11th IEEE International Conference on Embedded and Real-Time computing system and application*, 17-19 August 2005, Hong Kong

[5] J.SHIAN LI M.W. GUO, "Improving 802.11 Wireless TCP Performance with Adaptive Reed-Solomon Codes: An Experimental Study", *Journal Of Information Science And Engineering* 21, 1201-1211 (2005).

[6]M.F.Arnal, “Optimisation de la fiabilité pour des communications multipoint par satellite géostationnaire, *Thèse, Ecole Nationale supèrieure des télecommunications de paris,* 15 dec 2004.

[7] DVB, “Framing structure, channel coding and modulation for digital terrestrial television,” *ETSI EN 300* 744, vol. 4.1, January 2001

[8]. Lee H., ―A high speed, low complexity Reed-Solomon decoder for optical communications,‖ IEEE Transactions on Circuits and Systems II, PP. 461-465, 2005

[9] Bhawna Tiwari, Rajesh Mehra, “Design and Implementation of Reed Solomon Decoder for 802.16 Network using FPGA” 978-1-4673-1318, IEEE 2012.

[10]WiMAX Forum: ”Mobile WiMAX. Part I: A TechnicalOverview and Performance Evaluation,” August 2006.

[11] Peter J. Ashenden, “The Designer’s Guide to VHDL”, Second Edition, Morgan Kaufmann Publishers, 2004.